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EXAMINER	
COLEMAN, ERIC	

ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/672,440	PATEL ET AL.
	Examiner	Art Unit
	Eric Coleman	2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-45 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-3,5-17,21-25,26,27,29-32,34-39,44 and 45 is/are rejected.

7)☒ Claim(s) 4,18-20,28,33 and 40-43 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date No.2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claim 21 recites the limitation "the younger instruction, canceling the effect of the older of the two instructions" in claim 21. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3,5,6,9,11,12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ekner (patent No. 6,289,445).

5. Ekner taught the invention substantially as claimed including a data processing ("DP") system comprising:

During execution of an instruction on a computer, in response to an operation of the instruction calling for an architecturally-visible side-effect in an architecturally-visible storage location, storing a value (exception token) representative of an architecturally-visible representation of the side effect, a format of the representative value being different than architecturally-visible representation of the side effect and resuming the

execution without generating the architecturally-visible side effect (e.g., see figs. 6a,6b,7a,7b and col. 3, lines 23-43 and col. 5, line 61-col. 8, line 57 and col. 10, lines 29-53).

6. Ekner did not expressly detail (claims 1,9) the later writing of the architecturally-visible representation corresponding to the representative value into the architecturally visible storage location. Ekner, however taught later using the exception token for processing the side-effect or exception and then cleared (e.g., see col. 8, line 48-col. 11). Therefore one of ordinary skill would have been motivated to store a architecturally visible version of the token information in order for the system to process the exception routine especially since the exception token was cleared.

7. Further as to claim 2 since in at least one embodiment the exception is delayed when an exception token is stored in the exception register and when the architectural register that is paired to the exception register is read and does not contain valid data the exception register is read then clearly the read of the paired architectural register would have caused reading of the exception register and trigger the start of the exception processing and storing the architecturally visible representation (e.g., see col. 8, line 57-col. 10, line 53). Further as to claim 3 since in the profiling or debugging of a system such as Ekner maintaining a record of the exceptions that occurred would have been necessary one of ordinary skill would have been motivated to trigger storing the representation of the exception when the execution was completed. As to the storing the value in a temporary register (claim 5) since the exception registers are not

permanently assigned then clearly they comprised temporary registers (e.g., see col. 7, lines 49-64).

8. As per claim 6,12 Ekner taught the representative value stored in a non-addressable storage register (token register) and the process of the instruction only ceding control on an instruction boundary (e.g., see col. 8, lines 6-57). The operation of computers such as the one taught by Ekner was well known at the time of claimed invention to require from time to time debugging to continue operation. As to placing the token in the cache or main memory (claim 11) one of ordinary skill would have been motivated to store the exception token in cache or main memory especially when the exceptions would been tracked or logged or profiled for debugging the computer operation.

9. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ekner as applied to claim 1 above, and further in view of Song (patent No. 6,061,711) and Iyer.

10. Song taught the invention substantially as claimed including a data processing ("DP") system comprising:

a) Storing a context of a first process and loading a context of a second process to place the second process into execution, each context comprising a set of resources to be reloaded whenever a process associated with the context is reloaded for execution (e.g., see col. 1, lines 12-col. 2, line 60);

b) Instructions marked for execution in the pipeline to indicate whether or not a context switch may be performed at a boundary of the marked instruction (e.g., see col. 2, lines 47-60 and col. 10 line 7-col. 11, line 63).

11. Song did not expressly detail (claim 7) that at least some of the instructions a multi-stage execution pipeline of the computer maintaining results in storage resources outside the context resource set. Iyer however taught grouping exception handlers where some execution handlers held a superset execution data of other exception handlers and therefore data outside the context resource set (e.g., see col. 5, lines 41-65). This would have allowed for the establishing of a second exception.

12. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Song and Iyer. Both Song and Iyer were directed toward the problems of performing context switches in a DP system. One of ordinary skill would have been motivated incorporate the Iyer teachings of provding grouped exception handlers and maintaining data in groups where one group is superset of another group in order to allow one process to pass variables to another process area without copying variables and not affect the processing of third process (e.g., see col. 5, lines 41-67 of Iyer).

13. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Iyer and Ekner. The incorporation of teachings of the particular types of exceptions as taught by Ekner would have provided additional utility for the superset exception handler system of Iyer. One of ordinary skill would have been motivated incorporate the Iyer teachings of providing grouped exception handlers and maintaining data in groups where one group is superset of another group In the Ekner system in order to allow one process to pass variables to another process area without copying variables and not affect the processing of third process (e.g., see col. 5, lines 41-67 of Iyer).

14. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ekner as applied to claim 1 above, and further in view of Iyer (patent No. 6,481,007).

15. Iyer taught recognizing hardware execution of an instruction stream, recognizing a condition that is a superset of a condition whose occurrence is desired to be detected, and raising a first exception as a result of recognizing the superset condition; filtering the superset condition to determine whether the desired condition has occurred by grouping exception handlers where some execution handlers held a superset execution data of other exception handlers and therefore data outside the context resource set (e.g., see col. 5, lines 41-65). This allowed for the establishing of a second exception.

16. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Iyer and Ekner. The incorporation of teachings of the particular types of exceptions as taught by Ekner would have provided additional utility for the superset exception handler system of Iyer. One of ordinary skill would have been motivated incorporate the Iyer teachings of providing grouped exception handlers and maintaining data in groups where one group is superset of another group in order to allow one process to pass variables to another process area without copying variables and not affect the processing of third process (e.g., see col. 5, lines 41-67 of Iyer).

17. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ekner as applied to claim 9 above, and further in view of Alpert (patent No. 5,659,679).

18. Alpert taught recognizing an condition including exception condition, and in response, setting the processor into single-step mode; and taking single-step exception after executing the second instruction, and setting the processor out of single-step

mode in industry standard processor such as the Pentium (e.g., see col. 1, line13-col. 2, line 63). Also processor exceptions in processors that perform more than one task at a time such as the Pentium are well known to include conditions that affect another instruction such as writing to a location to read by the other instruction.

19. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Ekner and Alpert. One of ordinary skill would have been motivated to incorporate the Alpert teachings of single step mode in the Ekner teachings for providing efficient processing of the exceptions in the Ekner system.

20. Claims 13-14,16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Song (patent No. 6,061,711) in view of Iyer (patent No. 6,481,007)

21. Song taught the invention substantially as claimed including a data processing ("DP") system comprising:

a) Storing a context of a first process and loading a context of a second process to place the second process into execution, each context comprising a set of resources to be reloaded whenever a process associated with the context is reloaded for execution (e.g., see col. 1, lines 12-col. 2, line 60);

b) Instructions marked for execution in the pipeline to indicate whether or not a context switch may be performed at a boundary of the marked instruction (e.g., see col. 2, lines 47-60 and col. 10 line 7-col. 11, line 63).

22. Song did not expressly detail (claim 13) that at least some of the instructions a multi-stage execution pipeline of the computer maintaining results in storage resources outside the context resource set. Iyer however taught grouping exception handlers

where some execution handlers held a superset (claim 14) execution data of other exception handlers and therefore data outside the context resource set (e.g., see col. 5, lines 41-65). This would have allowed for the establishing of a second exception.

23. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Song and Iyer. Both Song and Iyer were directed toward the problems of performing context switches in a DP system. One of ordinary skill would have been motivated incorporate the Iyer teachings of provding grouped exception handlers and maintaining data in groups where one group is superset of another group in order to allow one process to pass variables to another process area without copying variables and not affect the processing of third process (e.g., see col. 5, lines 41-67 of Iyer).

24. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Song and Iyer as applied to claim 13-14 above, and further in view of Alpert (patent No. 5,659,679).

25. Alpert taught recognizing an condition including exception condition, and in response, setting the processor into single-step mode; and taking single-step exception after executing the second instruction, and setting the processor out of single-step mode in industry standard processor such as the Pentium (e.g., see col. 1, line13-col. 2, line 63). Also processor exceptions in processors that perform more than one task at a time such as the Pentium are well known to include conditions that affect another instruction such as writing to a location to read by the other instruction.

26. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Song and Alpert. One of ordinary skill would have been motivated to

incorporate the Alpert teachings of single step mode in the Song teachings for providing efficient processing of the exceptions that would have involved context switching in the Song system.

27. Claims 17,21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Song and Iyer as applied to claim 16 above, and further in view of Ekner (patent No. 6,289,445).

28. Ekner taught that during execution of an instruction on a computer, in response to an operation of the instruction calling for an architecturally-visible side-effect in an architecturally-visible storage location, storing a value (exception token) representative of an architecturally-visible representation of the side effect, a format of the representative value being different than architecturally-visible representation of the side effect and resuming the execution without generating the architecturally-visible side effect (e.g., see figs. 6a,6b,7a,7b and col. 3, lines 23-43 and col. 5, line 61-col. 8, line 57 and col. 10, lines 29-53).

29. Ekner did not expressly detail (claim 17) the later writing of the architecturally-visible representation corresponding to the representative value into the architecturally visible storage location. Ekner, however taught later using the exception token for processing the side-effect or exception and then (claim 21) cleared (e.g., see col. 8, line 48-col. 11). Therefore one of ordinary skill would have been motivated to store a architecturally visible version of the token information in order for the system to process the exception routine especially since the exception token was cleared.

Claim Rejections - 35 USC § 102

30. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

31. Claims 22,24,27,29 are rejected under 35 U.S.C. 102(e) as being anticipated by Iyer.

32. Iyer taught recognizing hardware execution of an instruction stream, recognizing a condition that is a superset of a condition whose occurrence is desired to be detected, and raising a first exception as a result of recognizing the superset condition; filtering the superset condition to determine whether the desired condition has occurred by grouping exception handlers where some execution handlers held a superset execution data of other exception handlers and therefore data outside the context resource set (e.g., see col. 5, lines 41-65). This allowed for the establishing of a second exception.

33. Iyer taught (claim 27,29) a monitoring condition comprising a memory reference to an address to a reference class (e.g., see col. 5, lines 28-col. 7, line 20).

Claim Rejections - 35 USC § 103

34. Claim 23,32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iyer as applied to claim 22,24,27,29 above, and further in view of Alpert.

35. Alpert taught (claims 23,32) recognizing an condition including exception condition, and in response, setting the processor into single-step mode; and taking single-step exception after executing the second instruction, and setting the processor out of single-step mode in industry standard processor such as the Pentium (e.g., see col. 1, line13-col. 2, line 63).This would require (claim 32) vectoring to a debug entry point. Also processor exceptions in processors that perform more than one task at a time such as the Pentium are well known to include conditions that affect another instruction such as writing to a location to read by the other instruction.

36. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Iyer and Alpert. One of ordinary skill would have been motivated to incorporate the Alpert teachings of single step mode in the Iyer teachings for providing efficient processing of the exceptions in the Iyer system.

37. Claim 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iyer as applied to claim 22,24,27,29 above, and further in view of Ekner.

Ekner taught that during execution of an instruction on a computer, in response to an operation of the instruction calling for an architecturally-visible side-effect in an architecturally-visible storage location, storing a value (exception token) representative of an architecturally-visible representation of the side effect, a format of the representative value being different than architecturally-visible representation of the side effect and resuming the execution without generating the architecturally-visible side effect (e.g., see figs. 6a,6b,7a,7b and col. 3, lines 23-43 and col. 5, line 61-col. 8, line 57 and col. 10, lines 29-53).

38. Ekner did not expressly detail (claim 25) the later writing of the architecturally-visible representation corresponding to the representative value into the architecturally visible storage location. Ekner, however taught later using the exception token for processing the side-effect or exception and then cleared (e.g., see col. 8, line 48-col. 11). Therefore one of ordinary skill would have been motivated to store a architecturally visible version of the token information in order for the system to process the exception routine especially since the exception token was cleared.

39. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Iyer and Ekner. The incorporation of teachings of the particular types of exceptions as taught by Ekner would have provided additional utility for the superset exception handler system of Iyer.

40. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iyer as applied to claim 24 above, and further in view of Song.

41. Song taught Storing a context of a first process and loading a context of a second process to place the second process into execution, each context comprising a set of resources to be reloaded whenever a process associated with the context is reloaded for execution (e.g., see col. 1, lines 12-col. 2, line 60); Instructions marked for execution in the pipeline to indicate whether or not a context switch may be performed at a boundary of the marked instruction (e.g., see col. 2, lines 47-60 and col. 10 line 7-col. 11, line 63).

42. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Song and Iyer. Both Song and Iyer were directed toward the problems of

performing context switches in a DP system. One of ordinary skill would have been motivated incorporate the Song teachings of marking instruction for execution and indicating whether or not a context switch may be performed to allow the system to reduce the amount of data to be saved at context switch time by selecting the optimum time to switch contexts (e.g., see col. 15, lines 2-35).

43. Claim 30,31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iyer as applied to claim 24 above, and further in view of Ekner.

44. Ekner taught (claim 30,31) the filtering software records the nature of the monitored condition including where there were multiple occurrences (e.g., see col. 3, lines 29-43).

45. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Iyer and Ekner. The incorporation of teachings of the particular types of exceptions as taught by Ekner would have provided additional utility for the superset exception handler system of Iyer.

Claim Rejections - 35 USC § 102

46. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

47. Claims 34,36,39,44,45 is rejected under 35 U.S.C. 102(b) as being anticipated by Alpert (patent No. 5,659,679).

48. Alpert taught (claims 34,36) recognizing an condition including exception condition, and in response, setting the processor into single-step mode; and taking single-step exception after executing the second instruction, and setting the processor out of single-step mode in industry standard processor such as the Pentium (e.g., see col. 1, line13-col. 2, line 63). Also processor exceptions in processors that perform more than one task at a time such as the Pentium are well known to include conditions that affect another instruction such as writing to a location to read by the other instruction. As per claim 39 instructions that write to registers wherein in one implementation the data is stored in one or more stacks (e.g., see col. lines 36-52 and col. 5, line 59-col. 6, line 5). Further as understood Alpert taught (claim 44) servicing a single-step exception including querying a debug touch record (e.g., see col. 6, lines 28-40). As per claim 45 Alpert taught an instruction for writing an interrupt enable flag of the computer (e.g., see col. 4, lines 21-37).

Claim Rejections - 35 USC § 103

49. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Alpert as applied to claim 34 above, and further in view of Ekner (patent No. 6,289,445).

50. Ekner taught the invention substantially as claimed including a data processing ("DP") system comprising:

a) During execution of an instruction on a computer, in response to an operation of the instruction calling for an architecturally-visible side-effect in an architecturally-visible storage location, storing a value (exception token) representative of an

architecturally-visible representation of the side effect, a format of the representative value being different than architecturally-visible representation of the side effect and resuming the execution without generating the architecturally-visible side effect (e.g., see figs. 6a,6b,7a,7b and col. 3, lines 23-43 and col. 5, line 61-col. 8, line 57 and col. 10, lines 29-53).

51. Ekner did not expressly detail (claim 35) the later writing of the architecturally-visible representation corresponding to the representative value into the architecturally visible storage location. Ekner, however taught later using the exception token for processing the side-effect or exception and then cleared (e.g., see col. 8, line 48-col. 11). Therefore one of ordinary skill would have been motivated to store a architecturally visible version of the token information in order for the system to process the exception routine especially since the exception token was cleared.

52. Claim 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alpert as applied to claim 36 above and further in view of Song (patent No. 6,061,711) and Iyer (patent No. 6,481,007)

53. Song taught a) Storing a context of a first process and loading a context of a second process to place the second process into execution, each context comprising a set of resources to be reloaded whenever a process associated with the context is reloaded for execution (e.g., see col. 1, lines 12-col. 2, line 60); b) Instructions marked for execution in the pipeline to indicate whether or not a context switch may be performed at a boundary of the marked instruction (e.g., see col. 2, lines 47-60 and col. 10 line 7-col. 11, line 63).

54. Song did not expressly detail (claim 37) that at least some of the instructions a multi-stage execution pipeline of the computer maintaining results in storage resources outside the context resource set. Iyer however taught grouping exception handlers where some execution handlers held a superset execution data of other exception handlers and therefore data outside the context resource set (e.g., see col. 5, lines 41-65). This would have allowed for the establishing of a second exception.

55. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Song and Iyer. Both Song and Iyer were directed toward the problems of performing context switches in a DP system. One of ordinary skill would have been motivated incorporate the Iyer teachings of providing grouped exception handlers and maintaining data in groups where one group is superset of another group in order to allow one process to pass variables to another process area without copying variables and not affect the processing of third process (e.g., see col. 5, lines 41-67 of Iyer). Further one or ordinary skill would have been motivated to incorporate the Song and Iyer teachings into the Alpert system inorder to provide means to process context switches that were detected in the Alpert system during debugging (e.g., see col. as 5, line 47-col. 6, line 49).

56. Claim 38 is rejected under 35 U.S.C. 103(a) as being unpatentable over Alpert as applied to claim 36 above and further in view Iyer (patent No. 6,481,007).

57. Iyer taught (claim 38) recognizing hardware execution of an instruction stream, recognizing a condition that is a superset of a condition whose occurrence is desired to be detected, and raising a first exception as a result of recognizing the superset

condition; filtering the superset condition to determine whether the desired condition has occurred by grouping exception handlers where some execution handlers held a superset execution data of other exception handlers and therefore data outside the context resource set (e.g., see col. 5, lines 41-65). This allowed for the establishing of a second exception.

58. Further one of ordinary skill would have been motivated to incorporate the Song and Iyer teachings into the Alpert system in order to provide means to process context switches that were detected in the Alpert system during debugging (e.g., see col. as 5, line 47-col. 6, line 49).

Allowable Subject Matter

59. Claims 4,18,19,20,28,33,40-43 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ooi (patent No. 5,043,878) disclosed a system with real-time checking of privilege levels and the systems state to allow access to internal access to internal resources of the system. (e.g., see abstract).

Anderson (patent No. 5,613,114) disclosed a DP system for custom context switching (e.g., see abstract).

Egcioglu (patent No. 5,625,835) disclosed a system for reordering memory operations and comprising delaying exceptions (e.g., see col. 8, lines 21-30).

Aurora (patent No. 6,119,218) disclosed a system for prefetching with an indication whether to handle an exception (e.g., see abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (703) 305-9674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC

ERIC COLEMAN
PRIMARY EXAMINER